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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

Application Number: 09/851,191  
Filing Date: May 08, 2001  
Appellant(s): PRITCHETT ET AL.

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Robert N. Rountree  
For Appellant

**EXAMINER'S ANSWER**

**MAILED**

MAR 07 2006

**GROUP 2800**

This is in response to the appeal brief filed on December 20<sup>th</sup>, 2005 appealing from the Office action mailed on September 21<sup>st</sup>, 2005.

**(1) Real Party in Interest**

A statement identifying the real part in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is correct.

**(4) Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The amendment after final rejection filed on September 1<sup>st</sup>, 2005 has been entered.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

**(8) Evidence Relied Upon**

Applicant Admitted Prior Art (AAPA)

Troster et al.; "An Interpolative Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array"; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477.

6,480,528	Patel	12-2002
4,665,532	Fukuda et al.	12-1987

### **(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 1-5, 7, 9 & 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Troster et al. (An Interpolative Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477).

Regarding to Claims 1-5, 7, 9 & 12-18, the Applicant Admitted Prior Art (AAPA) discloses an RF receiver apparatus embodied as an integrated circuit (Fig. 1 & Specification, Page 1, Background of Invention, lines 1-3) comprising a mixing circuitry for mixing an analog RF signal down to an analog IF signal (Specification, Page 3, lines 10-12 & Fig. 1, element 17); an analog IF-to-digital baseband converter, coupled to said mixer for converting said analog IF signal into a digital baseband signal, further comprising an analog-to-digital converter (ADC), a digital IF-to-baseband converter and a matched filter (Fig. 1, elements 12, 14, 15); and an output coupled to said analog IF-to-digital baseband converter for transmitting said

digital baseband signal (Fig. 1, element 18). The AAPA further discloses a baseband processing apparatus (digital signal processor) formed on a second integrated circuit for performing desired digital communications processing coupled to the output of the converter (Fig. 1, elements 13, 16 & Specification, Page 1, Background of Invention, lines 3-6 & Specification, Page 2, lines 1-2). The AAPA also discloses a matched filter (Fig. 1, element 15 & Specification, Page 2, lines 5-13). The AAPA further discloses the matched filter to include a decimator (Specification, Page 2, lines 14-21 & Fig. 2, element 15 & Specification, Page 3, lines 1-18). The AAPA also discloses an example of the digital IF-to-digital baseband converter to include a CORDIC (Coordinate Rotation Digital Computer) circuit (Fig. 2, element 14 & Specification, Page 2, lines 8-13 & Specification, Page 3, lines 1-18). The AAPA further discloses the receiver to include a mixing circuitry along with the ADC on the same chip (Specification, Page 3, lines 10-12 & Specification, Page 6, lines 10-12). However, the AAPA does not disclose the mixing circuitry and the analog IF-to-digital baseband converter circuitry to be implemented on the same integrated circuit.

Troster discloses a bandpass analog-to-digital (ADC) converter, implemented on a 1.2um BiCMOS Analog/Digital array, for a cellular radio mobile (systems) receiver (Abstract, Page 471, lines 1-8). Troster also discloses implementing the ADC wherein the input is an analog IF frequency signal and is converted to digital baseband signal (Page 472, Fig. 1 & Page 471, Section II, Converter Architecture, Right-hand column –to-Page 473, Section II, Converter Architecture, Left-hand

column). Troster also discloses implementing the converter architecture using BiCMOS technology used for the fabrication of the mixed array, which has been optimized for high performance analog/digital (mixed signal) applications and further optimized for prototyping of interfaces between high frequency analog signals and complex digital baseband signals (Page 473, Section III, BiCMOS Implementation, Right-hand column). Troster also discloses the a BiCMOS technology for a monolithic implementation on a single integrated circuit of mixed signal circuit components for processing high frequency analog signals and digital baseband signals (Page 475, Fig. 6 & Page 473, Section III, BiCMOS Implementation, Right-hand column & Page 475, Left-hand Column, Section "Floorplan" & Page 476, Left-hand column, Section V, Conclusion). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Troster teaches implementing a BiCMOS technology for the implementation of a mixed signal (analog/digital) circuit components and further implementing a bandpass analog IF-to-digital baseband converter and this can be implemented in the receiver as described in the AAPA so as to provide a monolithic integrated signal path from a high frequency signal to a baseband signal so as to provide high level monolithic integration desired for cellular mobile transceivers. Furthermore, the mixing circuitry is analog (component) and can be integrated on the monolithic integrated circuit, along with the other analog components.

2. Claim 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Troster et al. (An Interpolative

Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477) in further view of Patel et al. (6,480,528).

Regarding to Claim 6, the AAPA in view of Troster discloses an RF receiver apparatus embodied as an integrated circuit comprising a mixing circuit and an analog-to-digital baseband converter wherein the converter further comprises a filter as described above. However, the AAPA in view of Troster does not disclose the filter further including a quantizer.

Patel discloses a method and receiver for processing a desired signal wherein the desired signal is sampled, processed by a matched filter and then quantized (Abstract, lines 6-9, Column 2, lines 63-65 & Column 3, lines 39-41, 59-67 & Fig. 4-5). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Patel teaches implementing a quantizer for quantizing the matched filter output and this can be implemented in the RF receiver apparatus as described in the AAPA in view of Troster so as to provide a predetermined number of bits of resolution of the data, thus satisfying the limitation of the claim.

3. Claims 8, 10-11 & 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant Admitted Prior Art (AAPA) in view of Troster et al. (An Interpolative Bandpass Converter on a 1.2-um BiCMOS Analog/Digital Array; IEEE Journal of Solid-State Circuits; Vol. 28, No. 4; April 1993; Pages 471-477) in further view of Fukuda et al. (4,665,532).

Regarding to Claims 8, 10-11 & 19, AAPA in view of Troster discloses a RF receiver apparatus comprising a mixing circuitry, an analog IF-to-digital baseband signal converter and a baseband processing apparatus physically separate from the RF receiver apparatus as described above. However, AAPA in view of Troster does not disclose the analog IF-to-digital baseband converter to include a parallel-to-serial converter connected between said analog IF-to-digital baseband converter and said output, said parallel-to-serial converter providing serial formatted.

Fukuda discloses a parallel-to-serial converter for converting data in a parallel format (I & Q) into a serial format after demodulation of the received signal so as to recover the transmitted data in the desired (serial) format (Fig. 2, element 210 & Column 3, lines 29-42 & Column 4, lines 20-35). Fukuda further discloses a clock implemented in a parallel-to-serial converter and a serial-to-parallel converter (Fig. 5, element "CLK"). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Fukuda teaches a parallel-to-serial converter, and this can be implemented in the receiver as described in AAPA in view of Troster so as to provide a serial data stream received as transmitted by the transmitter, thus satisfying the limitation of the claim. Furthermore, the conversion of the received serial data, in the baseband apparatus, and converting the data to parallel format is a matter of design choice depending on the application and format of the data transmitted from the transmitter.

**(10) Response to Argument**

In regards to the arguments presented the AAPA discloses an RF receiver apparatus comprising a mixing circuitry, an analog IF-to-digital baseband converter, and an output as described in Claims 1, 9, 13 & 18. Each of these components **(individually)** and their functionality is disclosed in the AAPA as described below and in Paragraph 3 of the Final Rejection mailed June 28<sup>th</sup>, 2005.

The Applicant Admitted Prior Art (AAPA) discloses an RF receiver apparatus embodied as an integrated circuit (Fig. 1 & Specification, Page 1, Background of Invention, lines 1-3) comprising a mixing circuitry for mixing an analog RF signal down to an analog IF signal (Specification, Page 3, lines 10-12 & Fig. 1, element 17); an analog IF-to-digital baseband converter, coupled to said mixer for converting said analog IF signal into a digital baseband signal, further comprising an analog-to-digital converter (ADC), a digital IF-to-baseband converter and a matched filter (Fig. 1, elements 12, 14, 15); and an output coupled to said analog IF-to-digital baseband converter for transmitting said digital baseband signal (Fig. 1, element 18). The AAPA further discloses a baseband processing apparatus (digital signal processor) formed on a second integrated circuit for performing desired digital communications processing coupled to the output of the converter (Fig. 1, elements 13, 16 & Specification, Page 1, Background of Invention, lines 3-6 & Specification, Page 2, lines 1-2). The AAPA also discloses a matched filter (Fig. 1, element 15 & Specification, Page 2, lines 5-13). The AAPA further discloses the matched filter to include a decimator (Specification, Page 2, lines 14-21 & Fig. 2, element 15 &

Specification, Page 3, lines 1-18). The AAPA also discloses an example of the digital IF-to-digital baseband converter to include a CORDIC (Coordinate Rotation Digital Computer) circuit (Fig. 2, element 14 & Specification, Page 2, lines 8-13 & Specification, Page 3, lines 1-18).

**However, the AAPA does not disclose the mixing circuitry and the analog IF-to-digital baseband converter circuitry (as disclosed in the AAPA described above) to be implemented on the same integrated circuit.**

Therefore, the AAPA does disclose the mixing circuitry and the analog IF-to-digital baseband converter but not on the same integrated circuit. This specific limitation is disclosed in the Troster reference.

Troster discloses a bandpass analog-to-digital (ADC) converter, implemented on a 1.2um BiCMOS Analog/Digital array, for a cellular radio mobile (systems) receiver (Abstract, Page 471, lines 1-8). Troster also discloses implementing the ADC wherein the input is an analog IF frequency signal and is converted to digital baseband signal (Page 472, Fig. 1 & Abstract, lines 1-8 & Page 471, Section II, Converter Architecture, Right-hand column –to-Page 473, Section II, Converter Architecture, Left-hand column) {Interpretation: Referring to Figure 1, this figure discloses an interpolative bandpass ADC wherein the input is an analog IF signal “ $X_{IF}(t)$ ” which is digitized by the modulator loop “ $Y_k$ ” and is further down converted to baseband signals by the quadrature demodulator “I & Q”}. Troster also discloses implementing the converter architecture using BiCMOS technology used for the fabrication of the mixed array, which has been optimized for high performance

analog/digital (mixed signal) applications and further optimized for prototyping of interfaces between high frequency analog signals and complex digital baseband signals (Page 473, Section III, BiCMOS Implementation, Right-hand column). Troster also discloses the a BiCMOS technology for a monolithic implementation on a single integrated circuit of mixed signal circuit components for processing high frequency analog signals and digital baseband signals (Page 475, Fig. 6 & Page 473, Section III, BiCMOS Implementation, Right-hand column & Page 475, Left-hand Column, Section "Floorplan" & Page 476, Left-hand column, Section V, Conclusion). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that Troster teaches implementing a BiCMOS technology for the implementation of a mixed signal (analog/digital) circuit components and further implementing a bandpass analog IF-to-digital baseband converter and this can be implemented in the receiver as described in the AIPA so as to provide a monolithic integrated signal path from a high frequency signal to a baseband signal so as to provide high level monolithic integration desired for cellular mobile transceivers.

The Troster reference discloses (teaches) the implementation of analog/digital circuitry on the same monolithic integrated circuit. Troster further discloses a component such as an analog IF-to-baseband converter to be implemented on the integrated circuit wherein the input is analog and the output is digital. Furthermore, the mixing circuitry is analog (component) and can be integrated on the monolithic

integrated circuit, the application as disclosed in the Troster reference is cellular so as to provide a complete integrated circuit.

In Response to the Arguments presented in "Suggestion or Motivation to Combine" on Page 6 of the Brief that "Troster discloses in Figure 6 (page 475) a circuit that is equivalent to base band processor of Figure 1 of Appellant's admitted prior art", this is incorrect. Figure 6 on Page 6 of the Troster reference discloses the chip layout of the bandpass ADC, as described in Figure 1 of the Troster reference (as described in the above explanation), it is not the baseband processor. As noted above this chip acts as an interface portion to go from a high frequency signal to a baseband signal so as to provide monolithic integration of the complete signal path. Figure 1 of the Appellant's admitted prior art does not disclose down conversion (IF-to-BB) and ADC on the same chip as is disclosed in the Troster reference.

In Response to the Arguments presented in "Reasonable Expectation of Success" on Page 6 of the Brief that "Tröster et al. disclose an IF-to- baseband conversion circuit at Figure 6, page 475. This IF-to-baseband conversion circuit is equivalent to the IF-to-baseband conversion circuit 13 at Figure 1 of Appellants' admitted prior art." this is incorrect. Figure 6 on Page 6 of the Troster reference discloses the chip layout of the bandpass ADC, as described in Figure 1 of the Troster reference (as described in the above explanation), it is not the baseband processor. As noted above this chip acts as an interface portion to go from a high frequency signal to a baseband signal so as to provide monolithic integration of the complete signal path. Figure 1 of the Appellant's admitted prior art does not disclose

down conversion (IF-to-BB) and ADC on the same chip as is disclosed in the Troster reference.

In Response to the Arguments presented in "All Claim Limitations" on Page 8 of the Brief that the Examiner simply ignores the limitation of mixing an analog RF signal to an analog IF signal, this is incorrect. The AAPA discloses the mixing circuitry to be integrated with the ADC (Fig. 1, element 11 & Specification, Page 3, lines 10-12 & Specification, Page 6, lines 10-12). Furthermore, the Troster reference discloses implementing the chip as describe above to be implemented in various applications with varying frequency ranges (Page 475, Measurements & Page 476, Conclusion). Troster also discloses implementing the analog signal processing with bipolar high-frequency components (Page 475, Floorplan & Page 474, Fig. 4). Troster also discloses the BiCMOS technology implemented in the chip to be implemented for prototyping of interfaces between high frequency analog components and digital components (Page 473, BiCMOS Array). Troster also discloses analog components to include mixers (Page 471, left-column, Introduction, lines 11-16). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that mixing circuitry is analog (component) and can be integrated on the monolithic integrated circuit as described in Troster.

Art Unit: 2634

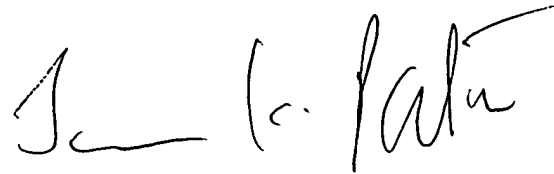
**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Sudhanshu C. Pathak



**JAY K. PATEL**  
**SUPERVISORY PATENT EXAMINER**

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Chieh M. Fan  
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